SPECIFICATIONS

MODEL	2551	4434	4448
General			
Function:	Counter	Latching Counter[2]	Latch
No. of Inputs:	12	32	48
Rate (MHz):	100	20 typical 30 instantaneous	150 MHz typical
Capacity:	24 bits or 48 bits by cascading channels[1]	24 bits (16,777,215 counts)	—
Double Pulse Resolution:	10 nsec	<30 nsec	8 nsec max., 6 nsec typ.
Inputs			
Signal:	–600 mV NIM into 50 Ω direct coupled. Reflections <10% with 1 nsec risetime. Min. width 7 nsec FWHM	Differential ECL (TTL factory option), 110 Ω pin-to-pin with Differential ECL, 560 Ω to ±5 V for TTL. Min. width 15 nsec	Differential ECL, 100 Ω direct coupled. <10% at 2 nsec risetime. Minimum width 4 nsec. Input sensitivity ±20 mV
Clear:	–500 mV NIM, 50 nsec clears all channels within 1 µsec or via CAMAC command	>20 nsec, NIM (TTL) will disable inputs for 100 nsec and clear scalers or via CAMAC command	–600 mV, >5 nsec, 2 nsec settling time after clear or CAMAC F(9) command
Inhibit/Veto/Gate:	–500 mV, >5 nsec must precede input by 10 nsec or via CAMAC inhibit	NIM (TTL) pulse or via CAMAC inhibit	–600 mV NIM, >3 nsec or via CAMAC inhibit[3]
Load:	n/a	>10 nsec NIM or TTL pulse or CAMAC F(16) will disable inputs for 220 nsec	n/a
Outputs			
Data Output:	Via CAMAC command	Via CAMAC command or via auxiliary bus	Via CAMAC command
Miscellaneous Output:	n/a	Total of 16 4434s may be integrated to auxiliary bus. This bus must end in an independent controller, permits addressed readout of content independent of CAMAC. Front-panel 24-pin connector	3 summing outputs from each 16 inputs groups. –100 mV ±10% presented for each register latched. Max. output –0.7 V (50 Ω) corresponds to 7 set registers. Risetime 3 nsec, delay of 9 nsec
Power Consumption:			
+6 V	1.2 A	3.1 A (ECL version) 2.8 A (TTL version)	400 mA
–6 V	100 mA	400 mA (ECL version) 40 mA (TTL version)	1.9 A

Notes:

1. By internal wire jumper option, even numbered channels may be cascaded with subsequent odd numbered channels to provide 48-bit channels. Any scaler generates LAM when 24th bit is set.
2. A set of side accessible switches allows the user to select different options as follows: LAD: Latching Disable; when ON the module works as a normal non-latching scaler. OVF: Overflow decides whether an overflow conditions occurs when bit 16 of any scaler is ON or when bit 24 is ON. LCO: Load and Clear at Overflow when ON. LOF: LAM at Overflow; a LAM is generated when at least one channel reaches the overflow set value. LRE: LAM at Readout Enable; a LAM is generated after a readout request. LDR: LAM Data Ready; a LAM is generated after a readout request and as long as there are data to be read. BAD: 4-bit Bus Address; defines module address in the auxiliary bus. VBR: Veto by Bus Readout; enables a veto of all scaler inputs during the loading of the auxiliary bus output registers (<200 nsec). NIM/TTL: Decides pulse standard accepted by inputs LOAD, CLEAR, and VETO.
3. Gate input delay: 2.5 nsec. Coincidence with 2.5 nsec and greater determined by input and gate pulse duration.